Separation frequency detection in a radar level gauge

Technical field

[0001] The present patent application relates to a separation frequency detector circuit for a radar level gauge. The present patent application further relates to a method for detection of a separation frequency in a radar level gauge. The invention can be used to generate an essentially chatter free difference frequency signal in fluid level sensing radar gauging systems.

Background of the invention

[0002] Non-contact range measurement pulse-echo radar systems for fluid level sensing in tanks and vats typically consist of a transmitter which is arranged to radiate short duration radio frequency (RF) bursts toward the surface of the product being stored in the tank or vat via a highly directional antenna. After a delay a receiver is gated at a particular point in time to receive energy which is reflected from the surface of the product. The timing of gating of the receiver is typically swept across a range of delays in a matter of milliseconds, such that a video output of the receiver can be provided as a scan like waveform. This waveform replicates occurring echoes on a real-time scale, corresponding to the physical distances represented by the echoes as the exact delay of a received echo pulse in relation to the transmitted pulse, i.e. the time of flight of the pulse, provides a measure of the distance to the reflecting object.

[0003] Highly accurate timing of the transmitted RF bursts and the gating of the receiver is necessary in order to be able to obtain high accuracy range information.

[0004] A precision digital pulse phase generator timing circuit is previously known through US 6,300,897 B1 which relates to a radar gauge adapted to sense fluid level in a tank and including a radar gauge circuit in which radar transmission and level sampling are controlled by a transmit frequency and a sample frequency respectively. A first frequency separation between first and second frequencies is controlled by a control input. The first and second frequencies can be divided to generate the transmit and sample frequencies, separated by a second frequency separation. At least one frequency difference is evaluated and the evaluation used to generate the control input, stabilizing the first frequency difference, and to correct the gauge output.

[0005] This timing circuit previously known through Fig. 8 of US 6,300,897 which is hereby incorporated by reference in its entirety, comprises a frequency difference circuit which receives the transmit clock frequency and the sample clock frequency and generates a frequency difference output. A polarity sensing circuit senses the polarity of the sample clock relative to the frequency difference output and generates a polarity, or sign, output. Both of these functions are suggested to be performed using low cost type 7474 clocked D flip flop circuits.

[0006] However, taking into account the timing requirements regarding setup and hold times for this kind of D flip-flop, the above separation frequency detector is not a very robust solution. If the signal at the D-input changes within the forbidden set-up and hold-time window, one of two reactions of the flip-flop can be observed:
1) The flip-flop works perfectly with no special behaviour;
2) The output of the flip-flop becomes unstable or "metastable".
If the output of a the flip-flop is "metastable", the output voltage is higher than the low-level-limit, but lower than the high-level-limit i.e. it is in the forbidden area between digital low and high. This situation can last less than 1ns, but could also last longer than 30ns. Also, the state the D flip-flop goes to after being metastable is random. The resulting behavior for the prior art circuit is that, during the time frame when the phase slip between the TX and RX clock is such that the setup/hold requirements are being violated, the output signal of the D flip-flop may change state each time it is being clocked. Thus, each edge of the Delta F signal may toggle or "chatter" with the frequency of the TX-clock for a duration corresponding to the sweep/phase slip time when the setup/hold time are being violated.

[0007] Another issue is that the TX and RX clock will always have some degree of phase noise. If the phase slip / separation frequency is slow enough the output may toggle or "chatter" simply due to the phase noise of the clock signals. However, the D flip-flop will only toggle for sure if the maximum differential phase noise between the two clock signals is greater than the sum of the setup and hold time for the flip-flop.

Summary of the invention

[0008] One object of the invention is to provide an improved separation frequency detector circuit for a radar level gauging system.

[0009] A further object of the present invention is to provide an essentially chatter free separation frequency detector circuit for a radar level gauging system which produces a distinct pulse the leading edge of which is synchronized with the first change of an original difference frequency leading edge without chatter.

[0010] A still further object of the present invention is to provide an essentially chatter free separation frequency detector circuit for a radar level gauging system which also produces a distinct pulse the trailing edge of which is synchronized with the first change of an original difference frequency trailing edge without chatter.

[0011] Another object of the present invention is to provide an essentially chatter free separation frequency detector circuit for a radar level gauging system which produces a restored difference frequency signal having the same duty cycle as an original difference frequency signal without chatter at the leading an trailing edges thereof.

[0012] Yet another object of the present invention is to provide an essentially chatter free separation frequency detector circuit for a radar level gauging system which is arranged to also provide an output signal indicative of the polarity of the difference frequency.

[0013] Briefly, a separation frequency detector circuit for a radar level gauge in accordance with a first embodiment of the present invention comprises a first circuit element which is arranged to receive a first clock frequency, and a second clock frequency, said first circuit element being arranged such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the second clock frequency, and a second circuit element arranged such that a predetermined value will be transferred to and held at an output Q thereof triggered by the output signal Q from said first circuit element, and said second circuit element further being arranged to clear said predetermined value from said output Q of said second circuit element a predetermined time period after being triggered, whereby an output is obtainable as a short pulse with a leading edge which will be synchronized with the first change of the original ΔF leading signal edge and no toggling will occur.

[0014] A further object of the present invention is to provide an improved method for detection of a separation frequency in a radar or laser rangefinder.

[0015] Briefly, a first embodiment of a method for detection of a separation frequency in a radar level gauge comprises the steps of: arranging a first circuit element to receive a first clock frequency, and a second clock frequency, and; arranging said first circuit element such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the second clock frequency, and; arranging a second circuit element such that a predetermined value will be transferred to and held at an output Q thereof triggered by the output signal Q from said first circuit element, and; arranging said second circuit element to clear said predetermined value from said output Q of said second circuit element a predetermined time period after being triggered, whereby a short pulse can be generated with a leading edge which will be synchronized with the first change of the original ΔF leading signal edge and no toggling will occur.

[0016] A still further object of the present invention is to provide an improved radar level gauge arranged to use microwaves for determining a level of a surface of a product stored in a container.

[0017] Briefly, a fist embodiment of the radar level gauge comprises a separation frequency detector in accordance with the present invention for precisely determining the separation frequency between said first and second clock frequencies of said radar level gauge for improved radar level gauging.

[0018] An advantage of the circuit and method in accordance with the present invention compared to prior art circuits and methods is that distinct and essentially chatter free detection of a separation frequency is obtainable using low cost standard components.

[0019] A further advantage of the circuit and method in accordance with the present invention is that a stable and essentially chatter free generation of output signal indicative of the polarity of the difference frequency is obtainable.

[0020] Further advantages and benefits of the present invention will become apparent from the following detailed description considered in conjunction with the accompanying drawings.

Description of drawings

[0021] In the following, the invention will be described in greater detail with reference to attached drawings, in which

[0022] Fig. 1 illustrates a typical signal definition, simple block diagram, of a timing generator for a radar level gauge.

[0023] Fig. 2 illustrates a prior art separation frequency detector for a radar level gauge.

[0024] Fig. 3 illustrates the prior art separation frequency detector of figure 2 with increased functionality for providing an output signal indicating the polarity of the separation frequency.

[0025] Fig. 4 illustrates a timing diagram of erroneous D flip-flop usage.

[0026] Fig. 5 shows an improved separation frequency detector in accordance with a first embodiment of the present invention.

[0027] Fig. 6 shows an explanatory timing diagram of the improved frequency detector of figure 5.

[0028] Fig. 7 illustrates a second embodiment of an improved separation frequency detector in accordance with the present invention.

[0029] Fig. 8 illustrates an improved separation frequency detector with completely restored separation frequency signal in accordance with a third embodiment of the present invention.

[0030] Fig. 9 illustrates the addition of a first alternative inclusion of a polarity sensing circuit element to the improved separation frequency detector of figure 8.

[0031] Fig. 10 illustrates the addition of a second alternative inclusion of a polarity sensing circuit element to the improved separation frequency detector of figure 8.

[0032] Fig. 11 illustrates an example application of a radar level gauge using microwaves for measuring a level of a surface of a product stored in a container.

[0033] Still other objects and features of the present invention will become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a definition of the limits of the invention, for which reference should be made to the appended claims. It should be further understood that the drawings are not necessarily drawn to scale and that, unless otherwise indicated, they are merely intended to conceptually illustrate the structures and procedures described herein.

Description of embodiments

[0034] In a radar fluid level sensing device, a transmitter generates a sequence of pulses which are directed towards a fluid surface, and the transmitter control output clock pulse TX control the transmitted pulses. A swept range gated receiver, triggered by the receiver control output clock pulse RX, receives reflected signals from the fluid surface whereby the fluid level can be determined.

[0035] The present invention is an enhancement of prior art related to a separation frequency detector which is typically used in timing generators based on controlling a fixed separation frequency between two oscillators. The invention could be used in any timing circuit based on controlling/measuring the separation frequency between two oscillators. Figure 1 illustrates a typical signal definition, simple block diagram, of such a timing generator. This timing generator has an SYS CLK input, which generates the Pulse Repetition Frequency PRF (TX clock). The Voltage Controlled Oscillator VCO CTRL input is an analog signal input controlling the frequency of the RX clock and thus also the separation frequency ΔF. The DELTA F output provides the separation frequency. The frequency of this signal is measured by a system processor and kept stable by adjusting the VCO CTRL signal accordingly. The PHASE output indicates the polarity of the DELTA F signal, i.e. indicates whether the RX frequency is higher or lower than the TX frequency. The TX output is the transmit clock and the RX output is the receive or sample clock.

[0036] In order for the timing generator to operate a function which detects the separation frequency ΔF, i.e. the separation frequency between the oscillator outputs TX and RX is required. In accordance with the prior art arrangement of US 6,300,897, the

separation frequency is obtained using a standard logic circuit known as an edge triggered flip-flop or D flip-flop.

[0037] The input of the D flip-flop is transferred to the output once each period of the TX clock, i.e. at the rising or falling edge of the TX clock signal depending on the type of flip-flop. However, the output of the D flip-flop will only change phase when the phase of the input signal, at the triggering edge of the TX clock input, changes 180 degrees. Thus, the Q output of the D flip-flop will be a signal with a frequency which is equal to the difference between the TX and RX frequencies. Another feature is that the phase of the output of the flip-flop will also be closely tied to the phase slip/difference between the TX and RX clocks, i.e. the separation frequency signal changes state when the phase slip between the TX and RX clocks is either zero or 180 degrees.

[0038] Figure 2 illustrates a prior art separation frequency detector 1 based on a standard D flip-flop (74HC74). The /CLR and /PRE inputs are kept at a logic high while the TX clock (TX CLK) is fed to the CLK input. The RX clock (RX CLK) is fed to the D input. The separation frequency ΔF (DELTA_F) is provided by the Q output of the D flip-flop.

[0039] To further increase the functionality of the prior art separation detector 1, it may be equipped with an output signal indicating the polarity of the separation frequency ΔF, just by adding an additional D flip-flop 2, as illustrated by the prior art arrangement of figure 3. The sample polarity detector 2 is connected as a flip-flop that stores the polarity of the sample clock (RX CLOCK) after the leading edge of the transmit clock (TX CLOCK) toggles the Q output of the difference frequency detector 1. The output of the transmit sample polarity detector 2 can be coupled to a microprocessor (not shown) to indicate whether the sample clock has a lower or higher frequency than the transmit clock. The polarity detector 2 resolves any ambiguity in the absolute value of the frequency difference.

[0040] A standard D flip-flop (74HC74) can be used also as the additional D flip-flop 2. The/CLR and /PRE inputs are kept at a logic high while the separation frequency ΔF at the Q output of the first D flip-flop 1 is fed to the CLK input of the additional D flip-flop 2. The RX clock is fed to the D input of the additional D flip-flop 2. The polarity or PHASE signal is provided by the Q output of the additional D flip-flop 2.

[0041] Assuming that the TX frequency is higher than the RX frequency, the PHASE signal will always be low since each time the additional flip-flop 2 is clocked by the rising edge of the ΔF signal the RX clock will always be high, due to the propagation delay from actual phase shift of the RX clock to the time when the output of the first flip-flop 1 changes state and vice versa when the TX frequency is lower than the RX frequency.

[0042] In theory and even for some specific manufacturers/batches of D flip-flops, a circuit such as the prior art circuit of figure 3 might work well. However, taking into account the requirements of setup and hold times for a practical D flip-flop, e.g. the standard D flip-flop (74HC74), the prior art separation frequency detector of figure 3 is not a very robust solution. If the signal at the D-input changes within the forbidden set-up and hold-time window, one of two reactions of the flip-flop can be observed:
1) The flip-flop works perfectly with no special behaviour;
2) The output of the flip-flop becomes unstable or "metastable".
If the output of a the flip-flop is "metastable", the output voltage is higher than the low-level-limit, but lower than the high-level-limit i.e. it is in the forbidden area between digital low and high. This situation can last less than 1ns, but could also last longer than 30ns. Also, the state the D flip-flop goes to after being metastable is random. The resulting behaviour for the prior art circuit is that, during the time frame when the phase slip between the TX and RX clock is such that the setup/hold requirements are being violated, the output signal of the D flip-flop 1 may change state each time it is being clocked. Thus, each edge of the Delta F signal may toggle or "chatter" with the frequency of the TX-clock for a duration corresponding to the sweep/phase slip time when the setup/hold time are being violated.

[0043] Another issue is that the TX and RX clock will always have some degree of phase noise. If the phase slip / separation frequency is slow enough the output may toggle or "chatter" simply due to the phase noise of the clock signals. However, the D flip-flop will only toggle for sure if the maximum differential phase noise between the two clock signals is greater than the sum of the setup and hold time for the flip-flop.

[0044] Assuming the following designations, ΔF [Hz] = Separation Frequency, t_s [s] = Setup time of the D flip-flop, t_H [s] = Hold time for the D flip-flop, PRF [Hz] = TX clock / Pulse Repetition Frequency, C [m/s] = 3E8 (Speed of Light), the time the D flip-flop is used out of specification corresponds to
[1]: $T_{PROBLEM} = [PRF \times (t_s + t_H)] / \Delta F$

[0045] An example D flip-flop (Fairchild 74AC74) has a typical $t_s + t_H$ of 1.0 ns at 25 deg C and a guaranteed minimum of 4.0 ns (-40 to +85 deg C). Thus the above expression [1] yields a worst-case persistence of roughly 230μs (occurring at each phase shift of the separation frequency signal) (ΔF=8Hz, PRF=1.8432 MHz) at room temperature, which is much longer than a measured persistence. Thus, the time the D flip-flop "chatters" is typically much less than the theoretical worst case persistence. Figure 4 illustrates a timing diagram of the erroneous D flip-flop usage.

[0046] The maximum real time delay of the RX clock versus the TX clock corresponds to 1/PRF (e.g. 542.5 ns which would render a maximum measuring range of 81,4 m for an associated radar level gauge). The time for the phase slip to cover the maximum real time delay is equal to $1/\Delta F$. Thus the worst case chatter equal to $T_{PROBLEM}$ would cause a

maximum measurement error corresponding to
[2]: Error [mm]=1000×[$T_{PROBLEM}$×ΔF]×C/[2×PRF]≤ 150 mm.
However, assuming the chattering time is equal from one period of the ΔF-signal to the succeeding period the error will be cancelled out.

[0047] In practice the measurement error caused by the above described potential malfunction may perhaps be acceptable, but some implementations of the generation of the PHASE signal and the detection of the separation frequency does not tolerate any chatter or glitches on the separation frequency signal. Note, that even without chatter on the ΔF signal the propagation delay of the first flip-flop 1 (se figure 3) needs to be longer than the setup time required for the second flip-flop 2.

[0048] Figure 5 shows an improved separation frequency detector in accordance with a first embodiment of the present invention as described above. In accordance with the present invention it is therefore suggested to use the original ΔF signal from the first D flip-flop to clock a second circuit element 3, such as a second edge triggered D flip-flop with a predefined logic input state and use a delayed version of the original ΔF signal edge to reset the output of the second flip-flop 3 a predetermined time period thereafter. Note that the /CLR and /SET control pins of the second D flip-flop 3 are independent of the CLK input and that they are not edge sensitive. The output will be a short pulse with a leading edge which will be synchronized with the first change of the original ΔF leading signal edge and no toggling will occur as long as the delay is selected to be significantly longer than the time defined by equation [1].

[0049] The separation frequency detector circuit for a radar level gauge according to figure 5 comprises a first circuit element 1, such as a first edge triggered flip-flop or D flip-flop, which is arranged to receive a first clock frequency, and a second clock frequency. The first circuit element 1 is arranged such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q of the first circuit element 1 once each period of the second clock frequency. A second circuit element 3, such as a second edge triggered flip-flop or D flip-flop, is arranged such that a predetermined value will be transferred to and held at an output Q of the second circuit element 3 triggered by the output signal Q from the first circuit element 1. The second circuit element 3 is further arranged to clear said predetermined value from the output Q of the second circuit element 3 a predetermined time period after being triggered.

[0050] The first clock frequency is preferably a sample clock frequency RX and the second clock frequency a transmit clock frequency. However, as will be obvious to the person skilled in the art, the first clock frequency can also be a transmit clock frequency TX and the second clock frequency a sample clock frequency RX, which will provide a corresponding output signal of inverted sign.

[0051] Figure 6 shows an explanatory timing diagram of the improved frequency detector of figure 5. Note that no false pulse will occur at the falling edge of the original ΔF signal since the second flip-flop will be held cleared by the delayed "/CLR" signal. The topmost diagram illustrates the output Q of the first circuit element 1 over time. The middle diagram illustrates the CLR signal provided to the second circuit element. The lowermost diagram illustrates the Q output of the second circuit element 3.

[0052] As shown in figure 7, in a second embodiment of an improved separation frequency detector, by applying essentially the same technique to both edges, i.e. rising and falling edge, of the original ΔF signal, two synchronized short pulses can be created. This is achieved through arranging a third circuit element 4, such as a third edge triggered flip-flop or D flip-flop with a predetermined logic input state, such that a predetermined value will be transferred to and held at an inverted output /Q thereof triggered by an inverted output signal /Q from said first circuit element 1. Said third circuit element 4 further being arranged to clear said predetermined value from said inverted output /Q of said third circuit element 4 a predetermined time period after being triggered. Thus, in a corresponding manner, the output will be a short pulse with a trailing edge which will be synchronized with the first change of the original ΔF trailing signal edge and no toggling will occur as long as the delay is selected to be significantly longer than the time defined by equation [1].

[0053] The two synchronized pulses obtainable by the arrangement of figure 7 may be used to, in turn, create a "restored" ΔF signal, which even has the same duty cycle as the original ΔF signal. An improved separation frequency detector with completely restored ΔF signal in accordance with a third embodiment of the present invention is shown in figure 8. Here a fourth circuit element 5, such as a fourth edge triggered flip-flop or D flip-flop with a predefined logic input state, is arranged such that the value of an inverted output signal from said second circuit element 3 will be transferred to and held at an output Q thereof. Said fourth circuit element 5 further being arranged to clear said value triggered by an inverted output /Q from said third circuit element 4.

[0054] Figure 9 illustrates the addition of a first alternative inclusion of a flip-flop 6 that stores the polarity of the first clock frequency after the leading edge of the second clock frequency toggles the Q output of the difference frequency detector. A fifth circuit element 6, such as a fifth edge triggered flip-flop or D flip-flop, is arranged to receive a first clock frequency, said fifth circuit element 6 being arranged such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the output signal Q from the second circuit element 3.

[0055] In figure 10 is shown a second alternative inclusion of a flip-flop 7 that stores the polarity of the first clock frequency after the leading edge of the second clock frequency toggles the Q output of the difference frequency detector. A sixth circuit element 7, such

as a sixth edge triggered flip-flop or D flip-flop, is arranged to receive a first clock frequency, said sixth circuit element 7 being arranged such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the output signal Q from the fourth circuit element 5.

[0056] Depending on the type of D flip-flop used the worst-case persistence may be quite long and the delayed /CLR signals of the improved circuits needs to be adjusted correspondingly. Delay can e.g. be achieved using a standard resistor 9 and capacitor 10 combination as shown in figures 5, 7, 8, 9 and 10. However, to long delays will/may cause noise on the slope of the delayed /CLR signal to false trigger the corresponding inputs of the second 3 and third 4 D flip-flops. This will cause the succeeding PHASE signal generating D flip-flop 6 to malfunction. The solution is either to insert a buffer with hysteresis 8, such as a Schmitt-trigger, prior to the /CLR inputs, as illustrated in figures 5, 7, 8, 9 and 10 or to use the "restored" ΔF signal to clock the "PHASE" D flip-flop 7, as illustrated in figure 10. The latter solution is preferred since it also increases the propagation delay and thus the setup margin for the "PHASE" D flip-flop.

[0057] A method for detection of a separation frequency for a radar level gauge in accordance with the present invention comprises the steps of: arranging a first circuit element 1, such as a first edge triggered flip-flop or D flip-flop, to receive a first clock frequency, and a second clock frequency; arranging said first circuit element 1 such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the second clock frequency; arranging a second circuit element 3, such as a second edge triggered flip-flop or D flip-flop, such that a predetermined value will be transferred to and held at an output Q thereof triggered by the output signal Q from said first circuit element 1; and arranging said second circuit element 3 to clear said predetermined value from said output Q of said second circuit element 3 a predetermined time period after being triggered.

[0058] In a further embodiment the method for detection of a separation frequency for a radar level gauge in accordance with the present invention comprises the additional steps of: arranging a third circuit element 4, such as a third edge triggered flip-flop or D flip-flop, such that a predetermined value will be transferred to and held at an inverted output /Q thereof triggered by an inverted output signal /Q from said first circuit element 1, and; arranging said third circuit element 4 to clear said predetermined value from said inverted output /Q of said third circuit element 4 a predetermined time period after being triggered.

[0059] In a yet further embodiment the method for detection of a separation frequency for a radar level gauge in accordance with the present invention comprises the additional steps of: arranging a fourth circuit element 5, such as a fourth edge triggered flip-flop or D flip-flop, such that the value of an inverted output signal from said second circuit element 3 will be transferred to and held at an output Q thereof, and; arranging said

fourth circuit element 5 to clear said value triggered by an inverted output /Q from said third circuit element 4.

[0060] In a still further embodiment the method for detection of a separation frequency for a radar level gauge in accordance with the present invention comprises the additional steps of: arranging a fifth circuit element 6, such as a fifth edge triggered flip-flop or D flip-flop, to receive a first clock frequency; arranging said fifth circuit element 6 such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the output signal Q from the second circuit element 3.

[0061] In yet a still further embodiment the method for detection of a separation frequency for a radar level gauge in accordance with the present invention comprises the additional steps of: arranging a sixth circuit element 7, such as a sixth edge triggered flip-flop or D flip-flop, to receive a first clock frequency; arranging said sixth circuit element 7 such that an instantaneous value of the first clock frequency will be transferred to and held at an output Q thereof once each period of the output signal Q from the fourth circuit element 5.

[0062] The present invention further relates to a radar level gauge using microwaves for measuring a level of a surface 16 of a product 12 in a container 11, an application of which radar level gauge is shown in figure 11. A container such as a tank 11 is used for storing the product 12. The product may be such as oil, refined products, chemicals and liquid gas, or may be a material in powder form. A radar 13 is attached to the roof 14 of the tank 11. A microwave beam is transmitted from the radar via an antenna 15 at the interior of the tank. The transmitted beam is reflected from the surface 16 of the product and is received by the antenna 15. By means of a comparison and evaluating of the time lap between transmitted and reflected beam in a measuring and controlling unit, a determination of the level of the product surface 16 is performed in a known manner. The microwave may be transmitted from the antenna as a free radiated beam or via a wave guide (not shown), which communicates with the product. The radar level gauge as shown in fig. 11 comprises an antenna 15 for transmitting microwaves towards the surface and receiving microwaves reflected by the surface 16. A microwave transfer medium, such as a waveguide or a coaxial cable, coupled at a first end to a measurement circuitry. The measurement circuitry is arranged to transmit and receive microwaves via the antenna 15. The measurement circuitry further being arranged to determine the level of the product 12 in the tank 11 based on the relation between transmitted and received microwaves. The measurement circuitry being arranged to determine the level of the product 12 in the tank 11 based on an analysis of a relation between microwaves transmitted at a second clock frequency, e.g. a pulse repetition frequency (TX CLOCK), and received microwaves sampled at a first clock frequency, e.g. a sample frequency (RX CLOCK). For the purpose of said determination the measurement circuitry includes a separation frequency detector, as described in detail above, for

precisely determining the separation frequency between said first and second clock frequencies of said radar level gauge, e.g. a difference (DELTA F) between said pulse repetition frequency (TX CLOCK) and said sample frequency (RX CLOCK).

[0063] In an additional embodiment the above described radar level gauge further comprises power supply circuitry for providing and distributing electrical power within the radar level gauge, and communication circuitry for communicating information including an indication of the level of the surface 16, and a two-wire interface for reception of electrical power to said power supply circuitry and for communication handled by said communication circuitry.

[0064] In yet a further embodiment the above described radar level gauge the power supply circuitry further includes energy storage circuitry.

[0065] The invention is not limited to the above-described embodiments, but may be varied within the scope of the following claims.

[0066] Thus, while there have been shown and described and pointed out fundamental novel features of the invention as applied to a preferred embodiment thereof, it will be understood that various omissions and substitutions and changes in the form and details of the devices illustrated, and in their operation, may be made by those skilled in the art without departing from the spirit of the invention. For example, it is expressly intended that all combinations of those circuit elements and/or method steps which perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Moreover, it should be recognized that structures and/or elements and/or method steps shown and/or described in connection with any disclosed form or embodiment of the invention may be incorporated in any other disclosed or described or suggested form or embodiment as a general matter of design choice. It is the intention, therefore, to be limited only as indicated by the scope of the claims appended hereto.